Name	Dr. Grish Phatak 
Designation	Scientist 'G' & Head, Electronics Packaging Division
Educational qualification	M. Sc. Physics with Electronics, (University of Pune, Pune) Ph.D in Microelectronics from Indian Institute of Technology, Bombay
Research area	• Thick film materials • Solder pastes • Electronics Packaging • Low Temperature Co-fired Ceramic (LTCC) fabrication and processes • Low Temperature Co-fired Ceramic (LTCC) Materials • Ceramic dielectric materials and composites • Ferrite materials and composites • Solid oxide fuel cells (SOFC) and its materials • Solder bumping • Lead-free electroplating and fine bumping
Recognised Awards/Honors/Fellow	• Life Member, MRSI • Life Member ISSS & Secretary, Pune Chapter • Member IEEE
Projects	**Ongoing Projects** • LTCC based devices for "Integrated low cost water sensors for real time water monitoring and decision making", IUSSTF, PI, Rs. 36.966 lakhs, June 2018-June 2021 • Development of Solid oxide fuel cells (SOFC) using LTCC technology, DST, PI, Rs. 212. lakhs, Nov. 2019 –Nov. 2022 • Development of LTCC based 3D Printing technology for low cost optoelectronic packaging, (Co-PI), Rs. 488.17 lakhs, Aug. 2020- Aug. 2023 **Completed Projects** **Number of projects completed till December 2014: 17 Nos** **Completed projects from Jan 2015 to till date:** • Prototype package fabrication, BARC, PI, Rs. 198.43 lakhs, Nov. 09-June 15 • General Purpose LTCC materials, DST & C-MET, PI, Rs. 651.58 lakhs, Nov. 12 – Nov. 16 • Microwave components on LTCC substrates, NPMASS, PI, Rs. 38.24 lakhs, June 14 – February 15 • Development of Magnetic sensors in LTCC (PI), BARC, Rs. 169.29

	Lakhs, Jan 2015-July 2018) • LTCC based Pressure Sensor, Eaton Technologies Pvt Ltd, PI, Rs. 35.63 lakhs, May 2015-July 2017 • Fabrication of multilayer RF circuits on LTCC (Co-PI), SAC, ISRO Rs. 45 Lakhs), June 2011- Nov. 2019 • Development of Sn-Ag-Cu based lead-free electrolyte for Surface finishing of PCBs, DST, Co-PI, Rs. 69.25 lakhs, May 2016- Nov. 2019 • Development of CNT-lead-free composites for Flip chip applications, Working group MeitY sponsored project, DST, Co-PI, Rs. 62.00 lakhs, Dec. 2014-March 2017 • Development of cryocoolers in LTCC, BRNS, Co-PI, Rs. 23.62 lakhs, May 2010- Jan. 2015
Publications/Patents	**Patents List (Past 5 years)** 1. A Non-conductive substrate with tracks formed by sand blasting, Girish Phatak, Shrikant Kulkarni, Vijaya Giramkar, Shany Joseph • US Patent Appl. No.15/542,567, Appln date 7th July 2017, Patent approved, NoA issued • European Patent Appl. No. 16737136.8, Appln date :18th July 2017 • Indian Patent Appl. No. 130/MUM/2015, Appln date: 13th Jan 2015 • PCT Appl. No.PCT/IB2016/050083, Appln date 8th Jan 2016 2. A Non-Conductive Substrate with Conductive Tracks Formed by Laser Ablation Method, Shany Joseph, Payal Bhawtankar, Adwait Shitole, Adwaita Jadhav, Vijaya Giramkar and Girish Phatak, Indian Patent Appl. No. 2335/MUM/2015, Appl Date: 18th June 2015, Publication Date: 23rd Dec 2016 3. Conductive solid oxide fuel cell electrolyte composition and a method for preparing the same Shrikant Kulkarni, Siddharth Duttagupta, Girish Phatak • Indian Patent Appl. No. 1573/DEL/2015, Appl. Date 1st June 2015 • PCT Appl. No.PCT/IB2016/050130PCT, Appl. Date 13th Jan 2016 • US Patent Appl. No.15/578,700US, Appl. Date 30th Nov. 2017 • European Patent Appl. No. 16802645.8, Appl. Date21st Dec.2017 4. Novel glass ceramic electrolyte for Low temperature solid oxide fuel cells Shrikant Kulkarni, Vijaya Giramkar, Siddharth Duttagupta, Girish Phatak • Indian Patent No. 335665, award date 20th April 2020 • PCT Appl. No.PCT/IB2016/050055PCT, Appl. Date 07th Jan 2016 • US Patent No. 10683236, Appl. No.15/542,212, granted on 20th April 2020, Appl. Date 7th July 2017 • European Patent Appl. No.16734953.9, Appl. Date 18th July 2017 5. A Low Temperature Co-fired Ceramic Substrate Miniature Fuel Cell and Manufacturing Method Thereof Shekhar Dimble, Shrikant Kulkarni, Tarkeshwar Patil, Ramesh Pushpagandhan, Girish Phatak and S. Duttagupta • Indian Patent Appl. No. 495/DEL/2015, Appl. Date 21st Feb 2015 • PCT Appl. No. PCT/IB2016/050134, Appl. Date 13th Jan 2016 • US Patent No. 10608267, Appl. No: 15/552,267, granted on 31st March 2020, Appl. Date 18th Aug. 2017 • European Patent Appl. No. 116751990.9, Appl. Date 12th Sept.2017 6. Counter flow heat exchanger for a miniature Joule-Thomson cryocooler,

	Milind D Atrey, Prasanna Gandhi and Girish Phatak, Appl. No. 2133/MUM/2010, Appl. Date 27th July 2010 7. Layered tough ceramics for armour applications, Kiran Akella and Girish Phatak, Indian Patent No 304258, Indian Patent Award Date 10th Dec. 2018 **Publications (Past 5 years)** 1. Study of glycine nitrate precursor method for the synthesis of gadolinium doped ceria ($Ce_{0.8}Gd_{0.2}O_{1.90}$) as an electrolyte for intermediate temperature solid oxide fuel cells, Shrikant Kulkarni, Siddhartha Duttagupta and Girish Phatak, RSC Advances, 4 (87) (2014) 46602–46612. 2. Sol-Gel Synthesis and Protonic Conductivity of Yttrium Doped Barium Cerate, Shrikant Kulkarni, Siddharth Duttagupta, Girish Phatak, Journal of Sol-Gel Science and Technology, 74 (1) (2015) 94-102. 3. Taguchi Design of Experiments for optimization of Ionic Conductivity in Nanocrystalline Gadolinium Doped Ceria, Shrikant Kulkarni, Siddharth Duttagupta, Girish Phatak, Ceramics International, 41(7), (2015)8973-8980. 4. Low-Temperature Sintering and Microwave Dielectric Properties of Zn_2SiO_4 Ceramic Added with Crystalline Zinc Borate, Varsha Chaware, Ravindra Deshmukh, Chetan Sarode, Suresh Gokhale & Girish Phatak, Journal of Electronic Materials, 44 (7), (2015) 2312-2320. 5. Study of stencil printing parameters for ball grid array formation at smaller pitch, Shrikant G. Kulkarni, Varsha A. Chaware, Girish J. Phatak, J. ISSS, 4 (1), (2015), 46-54. 6. Biochemical studies and characterization of immobilized alkaline phosphatases on carboxyl-functionalised Carbon Nano Tubes, Vijaya D. Giramkar, Dr. Girish J. Phatak and Sushma G. Sabharwal, International Journal of Scientific Research in Science and Technology (IJSRST), 5 (1), Print ISSN: 2395-6011 | Online ISSN: 2395-602X, 2018. 7. Effect of Graphite Content on the Polymer Based Resistor Paste for an Intergated Resistor on Printed Circuit Boards (PCB), M. Kolpe, S. Gosavi, G. Phatak, Journal of Nanoelectronics and Optoelectronics, 14 (7), (2019) 1030-1036.